



## **Phylinks Announces Working-First-Silicon for PHY-820: PCIe PHY with Leading-Edge DFT Features**

*New product line debuts; collaboration with ASIC Architect enables combination of silicon-proven PCIe PHY with link controller and IP verification by Avery Design*

**SAN FRANCISCO, Calif. – November 14, 2007** – Phylinks, Inc., an innovator of IP cores for the design of physical layer (PHY) high-speed serial interfaces, announced today that it has delivered working-first-silicon of its PHY-820 PCIe PHY at the .13u process technology node. The PHY is designed with Phylinks’ robust design-for-test (DFT) architecture with an extremely small footprint and low power consumption. The PHY-820 is the debut product in an upcoming lineup of high-speed mixed-signal IP with extensive DFT capabilities.

Phylinks teamed with ASIC Architect, Inc. to provide SoC designers with a complete PCIe solution that includes PCIe PHY, link controller, and sample software. Avery Design Systems Verification IP was used to verify the PHY-820 together with ASIC Architect controller, providing assurance for designers who need reliable interoperability to meet tight product deadlines.

“Together with ASIC Architect, we were able to forge a powerful PCIe PHY/MAC solution verified by Avery’s core-to-chip-level verification,” said Antony Sou, chief operating officer and founder of Phylinks. “Combined with our unrivalled expertise in mixed-signal DFT, this solution reduces risk for SoC designers and allows them to build higher-performance PCIe designs while minimizing design time.”

“Phylinks’ silicon-proven PCIe PHY is a perfect match for our high-speed PCIe link controller,” said Kishore Mishra, president and CEO of ASIC Architect, Inc. “With verified, seamless interoperability and powerful DFT features, this combination delivers a quick-to-market solution for designers with exceptional performance and power specifications.”

“The success of our collaboration with Phylinks and ASIC Architect is another example of how Avery provides assurance to designers at various stages of the design process, avoiding costly surprises at the implementation stage,” said Chilai Huang, president of Avery Design. “We will continue to work with IP vendors to ensure compatibility and interoperability in this very competitive sector.”

The Phylinks PHY-820 supports the high-performance PCI Express (PCIe) PIPE architecture designed for use in enterprise, desktop, mobile, communications and

embedded platforms. Phylinks' PCIe architecture is designed to support the PCI Express Base 2.0 specification (PCIe 2.0) in future IP designs.

### **Comprehensive Mixed-Signal DFT**

Traditionally, it has been difficult to test mixed-signal IP cores during debug or manufacturing. Phylinks has met these challenges with innovative DFT techniques that provide unprecedented assurance for SoC developers seeking market-beating, high-yield PCIe designs. Some of the DFT functionality in the PHY-820 includes:

- Extensive on-board test and diagnostics provide access for controlling and observing internal functions
- Full-speed PRBS self-test permits use of low-cost testers
- Internal parallel and serial data loopback options offer flexible testing options
- Self-checking PLL facilitates production testing
- Dedicated test pad provides analog coverage during characterization
- Scan-testable digital logic ensures accuracy

### **Pricing and Availability**

The Phylinks PHY-820 is available immediately. Customers may take advantage of Phylinks' innovative evaluation license, among the first of its kind in the mixed-signal arena. The license enables designers to evaluate IP cores prior to making a full licensing commitment. For more information please contact [sales@phylinks.com](mailto:sales@phylinks.com).

### **About Phylinks IP cores**

Phylinks IP cores are optimized for minimum area, low power, extensive testing, and interoperability with a variety of third-party solutions. This makes them ideal for use in the development of high-performance communications, PC, mass storage, optical and server applications. Phylinks IP cores are designed with a particular emphasis on test and manufacturing. Phylinks' innovative architecture effectively tackles the complex issues of testing high-speed mixed-signal designs. Phylinks cores are standard with full application support to facilitate rapid design-in, and include all necessary reference design, layout and simulation models, as well as IP documentation and characterization results.

### **About Phylinks**

Phylinks, Inc. provides a portfolio of IP Cores for the design of physical layer (PHY) high speed serial interfaces. Phylinks cores can be implemented in a variety of chip designs for use in advanced PCs, PC peripherals, servers, and 3G communications devices. Phylinks was founded in December 2005 by Antony Sou and Philip Hodgett – two experienced mixed-signal designers with over 40 years of combined experience. In 2006, Nabil Takla, a silicon valley entrepreneur who is also the CEO of Innovative Semiconductors, Inc., invested in Phylinks and joined the management team as CEO and Chairman of the Board. Phylinks has offices in Manchester UK, and San Francisco, California. For more information, visit [www.phylinks.com](http://www.phylinks.com).

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